Claims

The following is a copy of Applicants' claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~___~~"), as is applicable:

1. (Currently Amended) A direct current offset correction system, comprising:

direct current offset correction circuitry having an adjustable bandwidth; and

control logic configured to effect a bandwidth change of the direct current offset correction circuitry by effecting an increase in the bandwidth during a sleep mode of operation that precedes an idle mode of operation, said bandwidth change expediting at least one of a warm-up and settling time of the direct current offset correction circuitry.

2. (Original) The system of claim 1, wherein the direct current offset correction circuitry includes a switching network in communication with the control logic, said direct current offset correction circuitry including at least one of a low-pass filter having a first resistor and a first capacitor and a digital high pass filter.

3. (Original) The system of claim 2, wherein the switching network includes at least one of a second capacitor and a second resistor.

4. (Original) The system of claim 3, wherein the switching network, responsive to a signal from the control logic, enables the second capacitor to change an equivalent capacitance of the first capacitor, said change in equivalent capacitance effecting the bandwidth change.

5. (Original) The system of claim 3, wherein the switching network, responsive to a signal from the control logic, enables the second resistor to change an equivalent resistance of the first resistor, said change in equivalent resistance effecting the bandwidth change.

6. (Original) The system of claim 3, wherein the switching network, responsive to a signal from the control logic, enables the second resistor to change an equivalent resistance of the first resistor and the second capacitor to change an equivalent capacitance of the first capacitor, said change in equivalent capacitance and equivalent resistance effecting the bandwidth change.

7. (Original) The system of claim 3, wherein the digital high-pass filter, responsive to a signal from the control logic providing response speed information, includes filter coefficients that are selected based on the signal from the control logic to alter the bandwidth of the digital high-pass filter.

8. (Original) The system of claim 3, wherein the digital high-pass filter, responsive to a signal from the control logic providing one of a plurality of filter coefficients, alters the bandwidth of the digital high-pass filter.

9. (Original) The system of claim 1, further including a serial bus interface disposed between the control logic and the direct current offset correction circuitry.

10. (Original) The system of claim 1, wherein the control logic resides in at least one of a processor, memory, and a receiver system that includes the direct current offset correction circuitry.

11. (Original) The system of claim 1, wherein the control logic is configured to effect a bandwidth change of the direct current offset correction circuitry in response to detecting a change in mode of operation.

12. (Original) The system of claim 1, wherein the control logic is configured to effect a bandwidth change of the direct current offset correction circuitry in response to receiving a mode command.

13. (Canceled)

14. (Currently amended) The system of claim ~~13~~ 1, wherein the control logic is configured to effect a bandwidth change of the direct current offset correction circuitry by effecting a decrease in the bandwidth when settling of the direct current offset correction circuitry is complete.

15. (Currently amended) The system of claim 1, wherein the control logic is further configured to effect a bandwidth change of the direct current offset correction circuitry by effecting an increase in the bandwidth during a compressed mode ~~of operation of~~ operation, said bandwidth change expediting at least one of a warm-up and settling time of the direct current offset correction circuitry.

16. (Original) The system of claim 15, wherein the control logic is configured to effect a bandwidth change of the direct current offset correction circuitry by effecting a decrease in the bandwidth when settling of the direct current offset correction circuitry is complete.

17. (Original) The system of claim 1, wherein the direct current offset correction circuitry includes at least one of a variable resistor and a variable capacitor.

18. (Original) The system of claim 17, wherein the variable resistor, responsive to a signal from the control logic, changes resistance to effect the bandwidth change.

19. (Original) The system of claim 18, wherein the variable capacitor, responsive to a signal from the control logic, changes capacitance to effect the bandwidth change.

20. (Original) The system of claim 17, wherein the variable capacitor, responsive to a signal from the control logic, changes capacitance to effect the bandwidth change.

21. (Currently amended) A direct current offset correction system, comprising:

means for providing direct current offset correction; and

means for changing the bandwidth of the direct current offset correction means by effecting an increase in the bandwidth during a compressed mode of operation, said bandwidth change expediting at least one of a warm-up and settling time of the direct current offset correction circuitry.

22. (Original) The system of claim 21, wherein the means for changing the bandwidth is responsive to means for detecting a change in mode of operation.

23. (Original) The system of claim 21, wherein the means for changing the bandwidth is responsive to means for receiving a mode of operation command.

24 – 25. (Canceled)

26. (Currently amended) A method of operating a direct current offset correction system, comprising:

providing direct current offset correction circuitry that is configured with an adjustable bandwidth; and

changing the bandwidth of the direct current offset correction circuitry by effecting an increase in the bandwidth during a sleep mode of operation that precedes an idle mode of operation, said bandwidth change expediting at least one of a warm-up and settling time of the direct current offset correction circuitry.

27. (Original) The method of claim 26, wherein changing the bandwidth includes changing at least one of an equivalent capacitance of the direct current offset correction circuitry and an equivalent resistance of the direct current offset correction circuitry.

28. (Original) The method of claim 26, wherein changing the bandwidth includes changing a digital high-pass filter bandwidth.

29. (Original) The method of claim 28, wherein changing a digital high-pass filter bandwidth includes changing filter coefficient values of the digital high-pass filter.

30. (Original) The method of claim 26, wherein changing the bandwidth is responsive to at least one of detecting a change in mode of operation and receiving a mode command.

31. (New) A method of operating a direct current offset correction system, comprising:

providing direct current offset correction circuitry that is configured with an adjustable bandwidth; and

changing the bandwidth of the direct current offset correction circuitry by effecting an increase in the bandwidth during a compressed mode of operation, said bandwidth change expediting at least one of a warm-up and settling time of the direct current offset correction circuitry.

32. (New) The system of claim 21, wherein the means for changing the bandwidth further comprises:

means for effecting a bandwidth change of the direct current offset correction means by effecting an increase in the bandwidth during a sleep mode of operation that precedes an idle mode of operation, said bandwidth change expediting at least one of a warm-up and settling time of the direct current offset correction circuitry.